SUMMARY IRT/C2MI WORKSHOP

Monday 22 June			
8:30 - 10:30	**IRT/C2MI**	Session 1	*3D Packaging*
11:00 - 12:30		Session 2	*3D Technology*
12:00 - 13:30	Lunch		
14:00 - 15:45	**Common IRT/C2MI D43D**	Session 3	*3D Technology for Photonics*
16:15 - 18:00		Session 4	*3D CAD tools & Design*

IRT/C2MI & D43D WORKSHOP – 22 June, 2015

Paradigms for 3D integration

MONDAY, JUNE 22 2015

Morning Session is IRT/C2MI workshop only
Afternoon Session is shared between IRT/C2MI and D43D workshops

SESSION 1		3D Packaging
Chair : Didier Louis – IRT-CEA LETI, France		
8:30-9:00 a.m.	**Truly Hermetic Wafer Level Package Technology**	**Sebastien Michel -** Teledyne Dalsa Semiconductor, CA
9:00-9:30 a.m.	**Advanced packaging solutions**	**Eric Saugier -** STMicroelectronics, France
9:30-10:00 a.m.	**On the path towards scalable 3D integration by advanced packaging**	**Thomas Brunschwiler -** IBM Zurich, Germany
10:00-10:30 a.m.	**Enhanced TSV Last technology for heterogeneous integration : Hi-rel and power device, RF applications**	**Gilles Simon -**CEA-LETI, France
10:30-11:00 a.m.	**COFFEE BREAK**	

SESSION 2		3D Technology
Chair : Dominique Drouin – Univ. Sherbrooke, Canada		
11:00-11:30 a.m.	**Fine pitch assembly for 3D Integration – The 'finer' points**	**David Danovitch -** Univ. Sherbrooke, Canada
11:30-12:00 a.m.	**New opportunities in 3D integrations**	**Jean Michailos -** STMicroelectronics, France
12:00-12:30 a.m.	**Advanced silicon interposer**	**Severine Cheramy -** CEA-LETI, France
12:30-14:00 a.m.	**LUNCH BREAK**	

SESSION 3		3d Technology for Photonics & Characterization
Chair : Severine Cheramy – CEA-LETI, France		
14:00-14:25 p.m.	**Optical interconnect packaging for Silicon Photonic devices using existing microelectronic assembly infrastructure**	**Paul Fortier -** IBM, Canada
14:25-14:50 p.m.	**Silicon Photonics for high data rate applications : from chip to module**	**Stephane Bernabé -** CEA-LETI, France
14:50-15:15 p.m.	**Virtual Qualifications With Applications to 3Di**	**Julien Sylvestre –** Univ. Sherbrooke, Canada
15:15-15:40 p.m.	**Hybrid materials for packaging**	**Isabelle Bord-Majek -** IMS Bordeaux, France
15:45-16:15 p.m.	**COFFEE BREAK**	

SESSION 4		3D CAD tools & Design
Chair : Pascal Vivet – CEA-Leti, France		
16:15-16:40 p.m.	**A Modern Approach to Chip-Package-Board Co-Optimization**	**John Park -** Mentor Graphics, USA
16:40-17:05 p.m.	**CAD Methodology for design of 3D ICs, leveraging existing 2D design flows**	**Ravi Varadarajan –** Atrenta, USA
17:05-17:30 p.m.	**A novel EDA Flow for Automatic 3D Space Partitioning and 3D DRC for Smart System Solutions**	**Stefano Pettazzi** – Silvaco, UK
17:30-18:00 p.m.	**Die-stacking architecture for future GPU design**	**Yuan Xie -** Santa Barbara University, USA
19:00-23:00 p.m.	**D43D GALA DINNER**	